AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-38 (Cancelled)

Claim 39 (Currently Amended): An apparatus comprising:

a ~~plurality of inputs~~ set of input ports;

a FIFO storage buffer;

request logic coupling said ~~plurality of inputs~~ set of input ports to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory ~~is adapted to~~ concurrently ~~maintain~~ maintains a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports, wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports.

Claim 40 (Currently Amended): The apparatus of claim 39, wherein said memory includes:

a first entry ~~adapted to maintain~~ that maintains a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry ~~adapted to maintain~~ that maintains a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

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Claim 41 (Currently Amended): The apparatus of claim 40, wherein said memory includes:

a third entry ~~adapted to maintain~~ that maintains a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry ~~adapted to maintain~~ that maintains a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

Claim 42 (Currently Amended): The apparatus of claim 39, wherein said memory ~~adapted to maintain~~ maintains a data identifier for each pointer in said plurality of pointers.

Claim 43 (Previously Presented): The apparatus of claim 42, wherein each data identifier identifies a data source.

Claim 44 (Previously Presented): The apparatus of claim 39, wherein said memory is a content addressable memory.

Claim 45 (Previously Presented): The apparatus of claim 39, wherein said request logic and said storage buffer are included in a multiple port memory.

Claim 46 (Currently Amended): An apparatus comprising:

a ~~plurality of inputs~~ set of input ports;

a FIFO storage buffer;

request logic coupling said ~~plurality of inputs~~ set of input ports to said FIFO storage buffer, wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports; and

a memory in communication with said request logic, wherein said memory ~~is adapted to~~ concurrently ~~maintain~~ maintains a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports,

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wherein said memory ~~is adapted to maintain~~ maintains a data identifier for each pointer in said plurality of pointers, wherein each data identifier identifies a data source, and

wherein said memory includes:

a first entry ~~adapted to maintain~~ that maintains a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports, and

a second entry ~~adapted to maintain~~ that maintains a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

Claim 47 (Currently Amended): The apparatus of claim 46, wherein said memory includes:

a third entry ~~adapted to maintain~~ that maintains a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry ~~adapted to maintain~~ that maintains a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

Claim 48 (Previously Presented): The apparatus of claim 46, wherein said memory is a content addressable memory.

Claim 49 (Previously Presented): The apparatus of claim 46, wherein said request logic and said storage buffer are included in a multiple port memory.

Claim 50 (Currently Amended): A sink port comprising:

~~a plurality of data inputs;~~

a multiple entry point FIFO having a plurality of data inputs in communication with ~~said plurality of data inputs~~ a set of input ports to accept and store data; and

an output port coupled to said multiple entry point FIFO to receive said data from said ~~storage buffer~~ multiple entry point FIFO and transmit said data on a communications link.

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Claim 51 (Currently Amended): The sink port of claim 50, wherein said multiple entry point FIFO includes:

a FIFO storage buffer;

request logic coupling said plurality of data inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory ~~is adapted to~~ concurrently ~~maintain~~ maintains a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports.

Claim 52 (Currently Amended): The sink port of claim 51, wherein said memory includes:

a first entry ~~adapted to maintain~~ that maintains a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry ~~adapted to maintain~~ that maintains a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

Claim 53 (Currently Amended): The sink port of claim 52, wherein said memory includes:

a third entry ~~adapted to maintain~~ that maintains a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry ~~adapted to maintain~~ that maintains a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

Claim 54 (Currently Amended): The sink port of claim 51, wherein said memory ~~is adapted to maintain~~ maintains a data identifier for each pointer in said plurality of pointers.

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Claim 55 (Previously Presented): The sink port of claim 54, wherein each data identifier identifies a data source.

Claim 56 (Previously Presented): The sink port of claim 51, wherein said memory is a content addressable memory.

Claim 57 (Previously Presented): The sink port of claim 51, wherein said request logic and said storage buffer are included in a multiple port memory.

Claim 58 (Currently Amended): A cross-bar switch comprising:

a set of input ports to receive data packets; and

a set of sink ports in communication with said set of input ports to accept and forward said data packets, wherein a first sink port in said set of sink ports includes:

a multiple entry point FIFO having a plurality of data inputs ~~adapted to~~ that store data from data packets accepted by said first sink port.

Claim 59 (Currently Amended): The cross-bar switch of claim 58, wherein said multiple entry point FIFO includes:

a FIFO storage buffer;

request logic coupling said plurality of data inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory ~~is adapted to~~ concurrently ~~maintain~~ maintains a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports.

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Claim 60 (Currently Amended): The cross-bar switch of claim 59, wherein said memory includes:

a first entry ~~adapted to maintain~~ that maintains a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry ~~adapted to maintain~~ that maintains a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

Claim 61 (Currently Amended): The cross-bar switch of claim 60, wherein said memory includes:

a third entry ~~adapted to maintain~~ that maintains a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry ~~adapted to maintain~~ that maintains a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

Claim 62 (Currently Amended): The cross-bar switch of claim 59, wherein said memory ~~is adapted to maintain~~ maintains a data identifier for each pointer in said plurality of pointers.

Claim 63 (Previously Presented): The cross-bar switch of claim 59, wherein said memory is a content addressable memory.

Claim 64 (Previously Presented): The cross-bar switch of claim 59, wherein said request logic and said storage buffer are included in a multiple port memory.

Claim 65 (Previously Presented): The cross-bar switch of claim 59, wherein said request logic and said storage buffer are included in a multiple port memory.

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Claim 66 (Previously Presented): The cross-bar switch of claim 58, wherein each sink port in said set of sink ports includes:

a multiple entry point FIFO having a plurality of data inputs.

Claim 67 (Previously Presented): The cross-bar switch of claim 58 further including:

a set of data rings in communication with said set of input ports and said set of sink ports.

Claim 68 (Previously Presented): The cross-bar switch of claim 67, wherein said multiple entry point FIFO includes a data input for each data ring in said set of data rings.

Claim 69 (Previously Presented): The cross-bar switch of claim 67, wherein said first sink port snoops data packets on each data ring in said set of data rings and determines whether to accept a first data packet based on a set of criteria, wherein said set of criteria includes:

said first sink port having sufficient storage space for storing said first data packet,

said first sink port supporting a destination targeted by said first data packet,

and

a total number of packets being received by said first sink port not exceeding a predetermined number of packets.

Claim 70 (Previously Presented): The cross-bar switch of claim 67, wherein said first sink port includes:

a ring interface coupled to said set of data rings to accept data from a plurality of sources and supply said data on a plurality of outputs;

said multiple entry point FIFO in communication with said plurality of outputs on said ring interface to receive and store said data from said ring interface; and

an output port coupled to said multiple entry point FIFO to receive data from said multiple entry point FIFO and transmit said data from said multiple entry point FIFO on a communications link.

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Claim 71 (Previously Presented): A method for a sink port in a cross-bar switch to collect data in a FIFO, said method comprising the steps of:

(a) accepting data from a first data packet, wherein said data accepted in aid step (a) is a subset of said first data packet;

(b) storing said data from said first data packet in a said FIFO;

(c) accepting data from a second data packet, wherein said data accepted in aid step c is a subset of said second data packet;

(d) storing said data from said second data packet in said FIFO.

Claim 72 (Previously Presented): The method of claim 71, wherein said first data packet originates from a first source and said second data packet originated from a second source.

Claim 73 (Previously Presented): The method of claim 71, further including the steps of:

(e) determining that said data accepted in said step (a) includes a first line of said first data packet;

(f) allocating a first location in said FIFO for storing data from said first data packet;

(g) determining that said data accepted in said step (c) includes a first line of said second data packet; and

(h) allocating a second location in said FIFO for storing data from said second data packet.

Claim 74 (Previously Presented): The method of claim 73, wherein said step (f) includes the steps of:

(1) creating a first pointer to said first location; and

(2) creating a first tag identifying said first data packet.

Claim 75 (Previously Presented): The method of claim 74, wherein said step (h) includes the steps of:

(1) creating a second pointer to said second location; and

(2) creating a second tag identifying said second data packet.

Claim 76 (Previously Presented): The method of claim 75, wherein said first tag identifies a source of said first data packet and said second tag identifies a source of said second data packet.

Claim 77 (Previously Presented): The method of claim 73, further including the steps of:

(j) accepting additional data for said first data packet;

(k) determining that said additional data accepted in said step (j) does not include a first line of said first data packet;

(l) identifying a position in said first location in said FIFO for storing said additional data from said first data packet;

(m) accepting additional data for said second data packet;

(n) determining that said additional data accepted in said step (m) does not include a first line of said second data packet; and

(o) identifying a position in said second location in said FIFO for storing said additional data from said second data packet.

Claim 78 (Previously Presented): The method of claim 77,

wherein said step (l) includes the step of:

(1) retrieving a pointer to said position in said first location, and wherein said step (o) includes the step of:

(2) retrieving a pointer to said position in said second location.

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Claim 79 (Previously Presented): The method of claim 73, further including the steps of:

(p) accepting additional data for said first data packet;

(q) determining that said additional data accepted in said step (p) includes a last line of said first data packet;

(r) purging a pointer to a position in said first location in said FIFO;

(s) accepting additional data for said second data packet;

(t) determining that said additional data accepted in said step (r) includes a last line of said second data packet; and

(u) purging a pointer to a position in said second location in said FIFO.

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